Comprehensive Power Integrity Analysis of 2.5DIC Design

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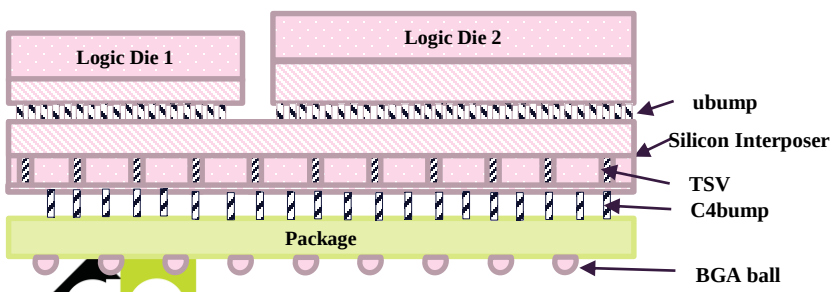
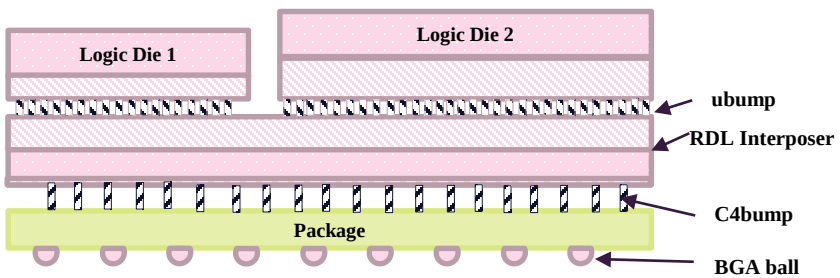
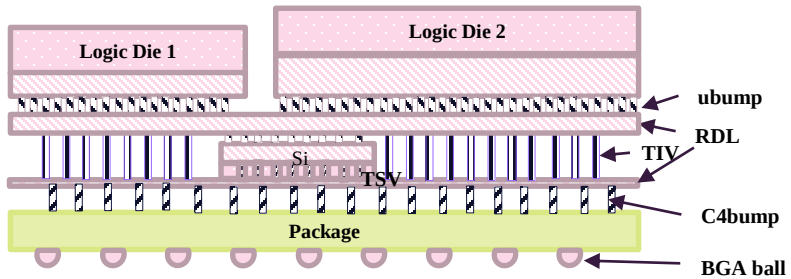
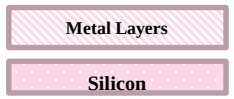
Motivation

- **Super complex 2.5DIC design**
  - SoC dies, memory, silicon bridges share multiple power/ground domains, operating frequency/scenarios are very complex
  - Interposer size can achieve thousands of square millimeters
  - Total power consumption in the kilowatt class
  - Overall size of power delivery network(PDN) can exceed hundreds of Billion Nodes/Resistors!
- **Power shared between multiple SoC dies, memories, RDL, silicon bridges and package**
  - Power noise can propagate across all these components
  - Rapidly changing workloads require the PDN to be able to respond quickly and maintain voltage stability
- **Cost-effectiveness management**
  - Super large power grid layout requires increased routing resources
  - Can no longer reserve a margin like the traditional way
- Need a precise approach to **predict/analyze the entire 2.5DIC PDN quality** and accurately capture coupling effects between each component **at both prototyping and sign-off stage**



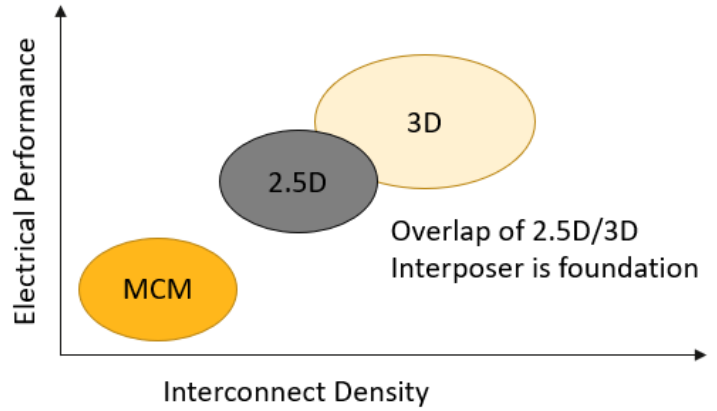


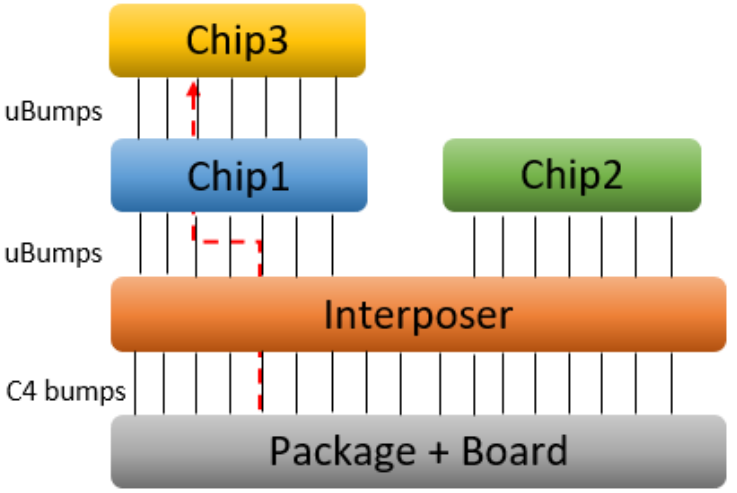




Motivation

- Critical decisions on topology and placement are need to be made at an early stage
  - Requires fast, yet accurate, trade-off studies for power integrity
  - Early-stage to sign-off full-path power integrity monitor
- Analysis must account for differences in:
  - Aspect ratio of features, fine features vs gross features in same model
  - Silicon ~1um, PKG (10s/100s ums) , BRD (mm)
  - ~10k connection -> Millions connections
- Concatenation of disparate databases
  - Must support variety of data formats
  - Must be fast, efficient, and scalable
  - Must be able to filter out the necessary context for the specific assessment, e.g. Silicon metal layers of focus, bumps, RDL, TSV, TIV, ports and specific power delivery
- Protection of IP, encryption of Inputs/Outputs

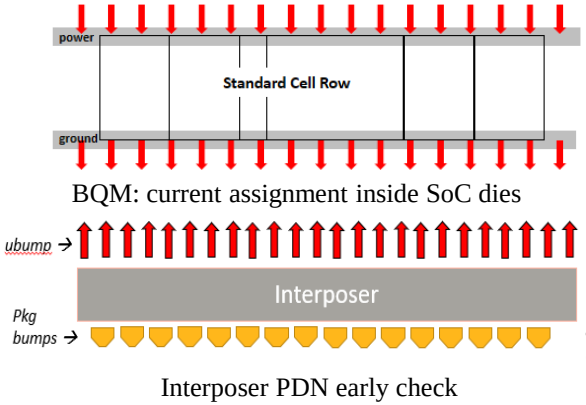




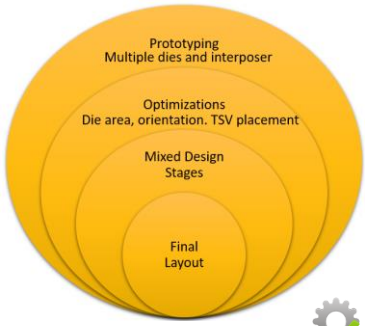
Main Idea

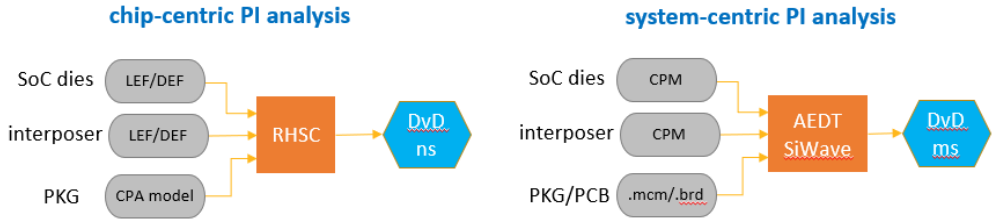
Engineering Goals

- Drive critical physical implementation decisions for power efficiency at prototyping stage, achieve best PPAC(Performance-Power-Area-Cost)
- Optimize most appropriate power design strategies, such as decoupling capacitor/TSV/TIV configuration strategy and power/ground planes, etc.
- Optimize Deep Trench Capacitor (DTC) configuration and placement on silicon bridges to ensure a stable power supply environment
- Fast, efficient, and scalable PDN analysis approach to analysis the entire super complex 2.5DIC system



Interposer PDN early check





Early-stage PDN Check

- For each SoC die, enable BQM(Build Quality Metric) check with preliminary collateral, finds weakness issues in entire power grid, even before instance placements
- Enable interposer PDN quality early check, detects weakness in grid density, TSV/TIV placement, DTC configuration and power/ground planes

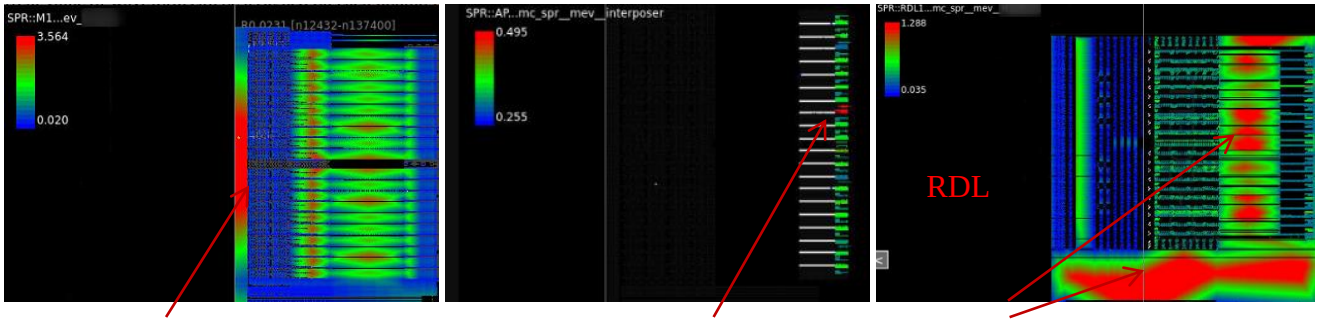
Signoff-stage PDN Validation

- **Chip-centric full 2.5DIC** system PI check**,** concurrent simulation takes into account the impact from shared P/G nets and DTC in silicon bridge, and detailed die2die coupling effects
- **System-centric full 2.5DIC** system PI check, accurate CPM(chip power model) based system analysis
- Leverage rollup or ROM(Reduced Order Model) technology for **faster TAT** & **lower memory** footprint

Interposer Static/Dynamic IR Analysis at Early Stage

- Interposer PDN analysis with preliminary collateral, current value or waveform can be assigned on each ubump to check Interposer IR/EM at prototyping stage
- Static/dynamic IR/EM hotspot heatmap help to check power grid density, bump placement, connection point placements and DTC contribution at early stage
- By increasing the DTC capacitance from 50nF to 100nF and optimizing the placement of the DTCs (placing them as close as possible to the load side), 7% reduction in dynamic voltage drop can be seen close to the load side

PG weakness detected at early stage

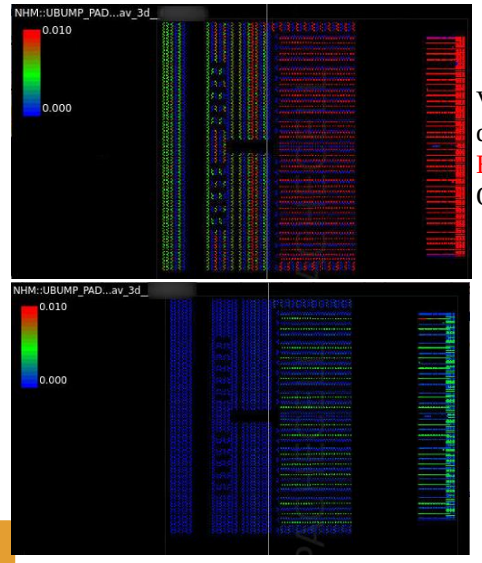


VSS weak connection due to missing VIA1

~500+AP bumps disconnected due to RV missing

RDL1 weak connection

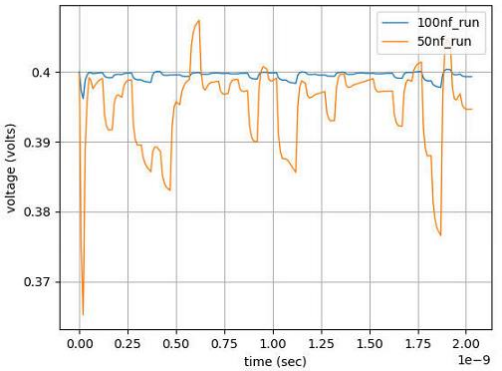
Dynamic IR heatmap
Before VS. After DTC Optimization



VDD2 node drop heatmap Before DTC Optimization

VDD2 node drop heatmap After DTC Optimization

Average Bump Voltage



VDD2 ideal voltage: 0.4V

***Before** DTC opt: worst drop 32mV*

***After** DTC opt: worst drop 4mV*

Worst IR drop diff: 7%

Allow SoC dies and interposer to iterate their PDN separately, streamlining and accelerating early cross-design team delivery

Quickly detect if interposer/silicon bridge meets the dynamic PI spec at bumps/TSV/TIV, etc.

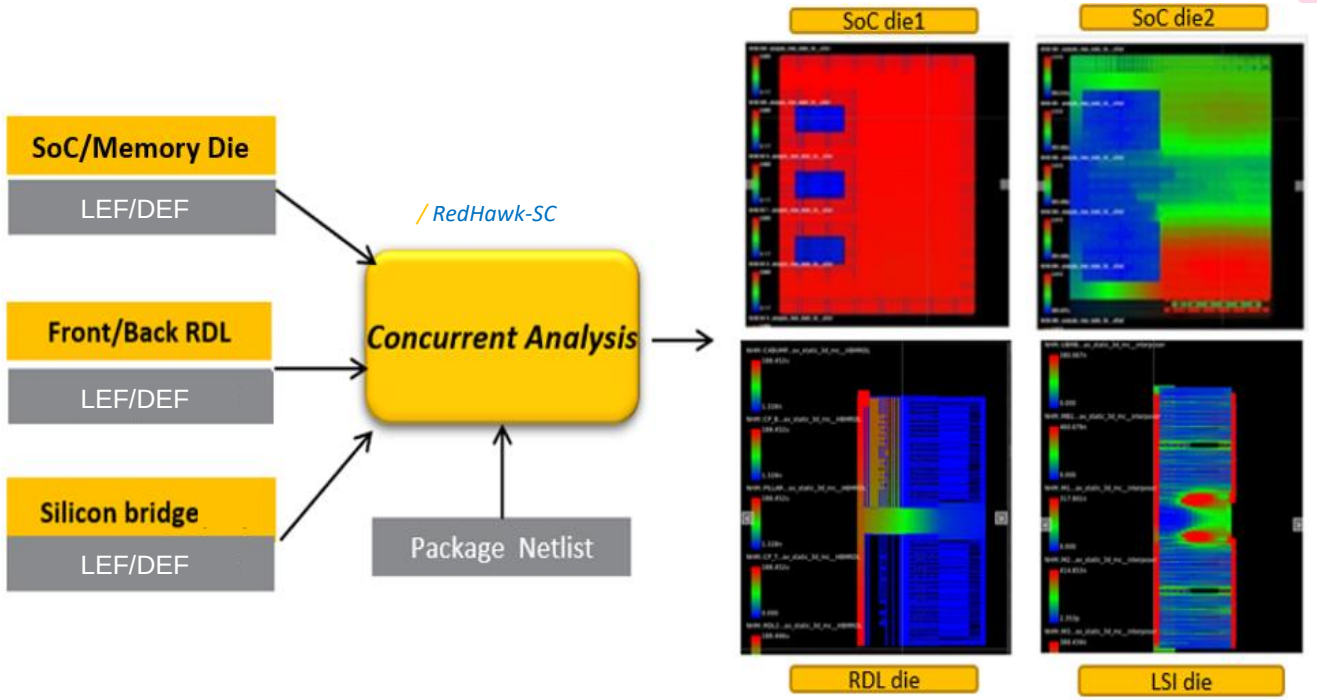
Provides guidance for SoC dies on dynamic bump fluctuation

Evaluate proper DTC capacitor placement and quantity at an early stage

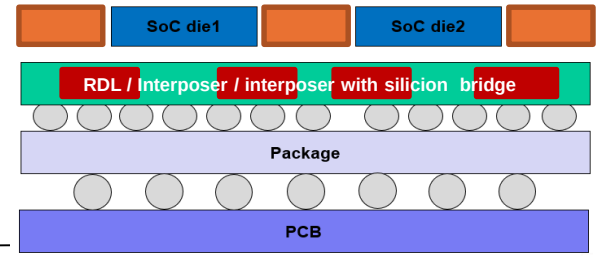
C_{DTC} & C_{die} → PDN System Response → APR Rule & Die Area Spec

Optimal PDN, early

Multi-die Large PDN Power Analysis at Sign-off Stage



Data Inputs



SoC data:
DEF/LEF, APL,
LIB, SPEF etc.

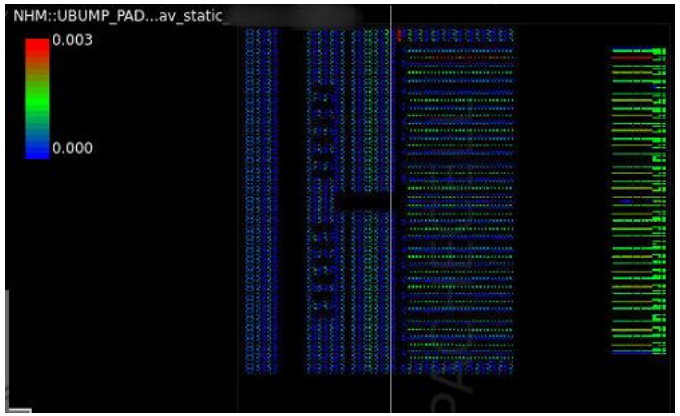
CP(µBump) : Location file and parasitics

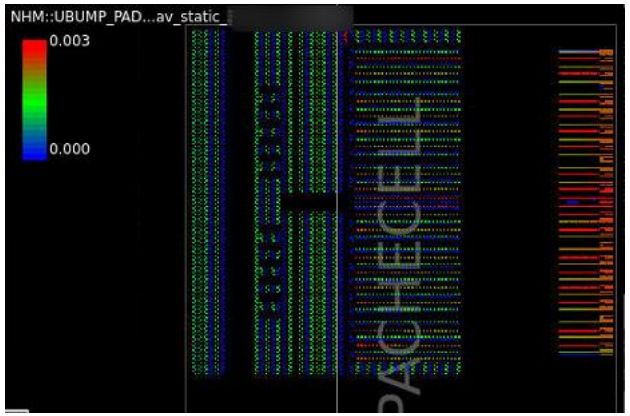
Interposer data:
DEF/LEF. LIB, SPEF etc.

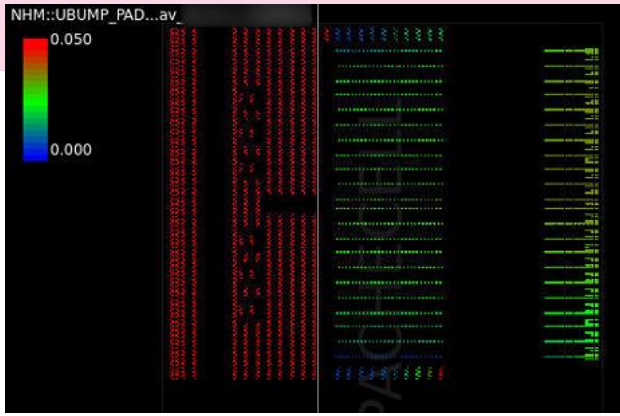
C4 Bump: Location file and parasitics

- **Multi SoC dies, memories, RDL, silicon bridges and package** are analyzed **simultaneously** with big data EDA tool
- Analysis use the model accordingly
  - All chiplets use DEF
  - Master chiplets use DEF, cloned chiplets use reduced model
- Leverage **vectored** or **vectorless** activities information to ensure worst case power consumption analyses
- Enable current density-based DC EM & RMS EM checking on the entire 2.5DIC design
- Siloed design groups have a common workflow: offchip <-> onchip

Package-aware Interposer PDN check







IR drop:
VDD1: 11.3uV
VDD2: 8.3mV
VSS: 3.4mV

Static run w/o pkg

Worse Static IR

IR drop:
VDD1: 42.6uV
VDD2: 10mV
VSS: 4.3mV

Static run w/ pkg

IR drop:
VDD1: 0.6mV
VDD2: 25.5mV
VSS: 28mV

Dynamic run w/o pkg

Worse Dynamic IR

IR drop:
VDD1: 142mV
VDD2: 183mV
VSS: 525mV

Dynamic run w/ pkg

demo case results

- Aids in early identification of risks and deficiencies in package, help package design optimization with minimize effort
- Through static SoC bump current-aware & package aware DC IR simulation of interposer, large resistance issue due to weak connection of the VDD net on the package is detected
- Through dynamic SoC bump current-aware & package aware transient hotspot simulation of interposer, high dynamic voltage drop observed on the interposer led to the discovery of a localized large inductance problem caused by routing congestion and fragmented routing on the package

different currents at bump
(of different RC values and scenarios)

differnernt IR drop at bump

Power Spec

Summary

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Summary

- It is important to perform power integrity simulation at the early design stage to establish the decoupling capacitor configuration strategy for chip/interposer/package level, the multi-layer power and ground planes, and to predict potential problems and adjust the PDN design strategy with the lowest cost
- Silicon Bridges not only help to realize high-density interconnects but also provide significant advantages in terms of power integrity for the 2.5DIC design
- Extending the power and ground planes on the silicon bridge directly near each functional module reduces voltage drop and noise and enhances power supply stability
- Placing more DTC on the silicon bridge close to the load point enables fast response to transient current changes and maintains a stable power supply environment
- Static/Dynamic SoC bump current-aware & package parasitic aware DC/AC IR simulation of interposer enable early detection of risks and deficiencies in package
- Faster TAT and excellent scenario coverage of the big data EDA tool ensure the design schedule

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